

	L #	Hits	Search Text	DBs
1	L1	570	(renam\$3 reorder\$3) near20 pipelin\$3	USPAT; US-PGPUB
2	L2	29331	(dependen\$3 conflict\$3) near10 (bit flag tag field)	USPAT; US-PGPUB
3	L3	1	1 near99 2	USPAT; US-PGPUB
4	L4	163	1 and 2	USPAT; US-PGPUB
5	L5	49	(renam\$3 reorder\$3) near20 pipelin\$3	EPO; JPO; DERWENT; IBM_TDB
6	L6	4535	(dependen\$3 conflict\$3) near10 (bit flag tag field)	EPO; JPO; DERWENT; IBM_TDB
7	L7	2	5 and 6	EPO; JPO; DERWENT; IBM_TDB

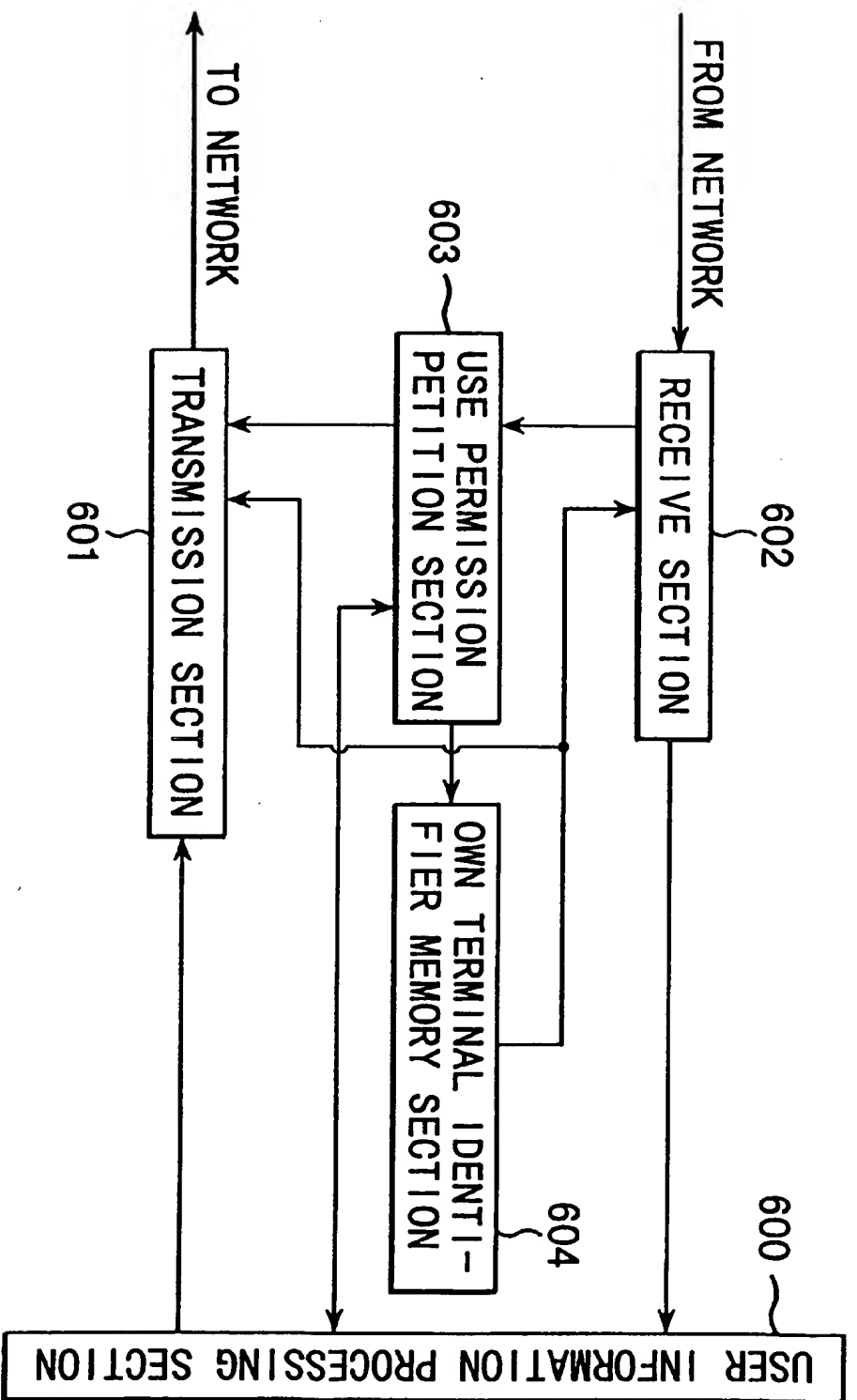


FIG. 14

	Docum ent ID	U	Title	Current OR
1	EP 70976 9 A	<input type="checkbox"/>	Pipeline microprocessor capable of issuing and executing multiple instructions - performs source operand dependency analysis, register re=naming and provides rapid pipeline recovery for microprocessor issuing and executing multiple instructions out of order in single machine cycle	
2	EP 43386 4 A	<input type="checkbox"/>	Hardware pipeline breaks minimiser - minimises hardware pipeline breaks using software scheduling techniques during compilation	

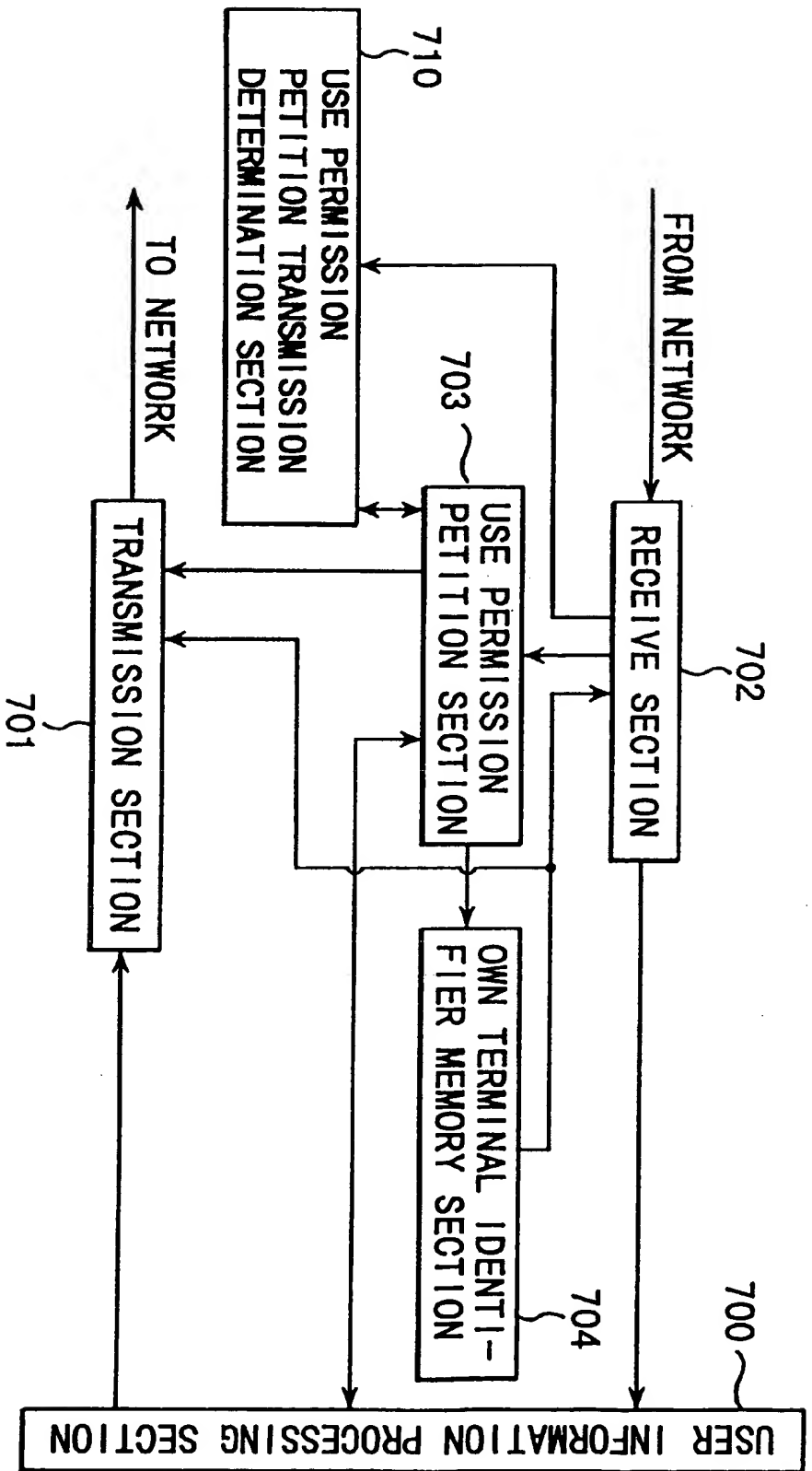


FIG. 15

	Docum ent ID	U	Title	Current OR
1	US 20030 21724 9 A1	<input type="checkbox"/>	Method and apparatus for virtual register renaming to implement an out-of-order processor	712/217
2	US 20030 20867 2 A1	<input checked="" type="checkbox"/>	Method and system for pipeline reduction	712/200
3	US 20030 20866 5 A1	<input checked="" type="checkbox"/>	Reducing data speculation penalty with early cache hit/miss prediction	711/169
4	US 20030 18254 2 A1	<input checked="" type="checkbox"/>	Method and apparatus for controlling execution of speculations in a processor based on monitoring power consumption	712/235
5	US 20030 15436 4 A1	<input checked="" type="checkbox"/>	MECHANISM FOR INSTRUCTION DATA FORWARDING IN A PIPELINE PROCESSOR	712/218
6	US 20030 14986 5 A1	<input checked="" type="checkbox"/>	Processor that eliminates mis-steering instruction fetch resulting from incorrect resolution of mis-speculated branch instructions	712/244
7	US 20030 14986 2 A1	<input checked="" type="checkbox"/>	Out-of-order processor that reduces mis-speculation using a replay scoreboard	712/217
8	US 20030 13571 4 A1	<input checked="" type="checkbox"/>	Method and apparatus for pre-processing instructions for a processor	712/217
9	US 20030 12640 6 A1	<input checked="" type="checkbox"/>	Stick and spoke replay	712/200
10	US 20030 04366 5 A1	<input checked="" type="checkbox"/>	LOW-POWER CIRCUIT STRUCTURES AND METHODS FOR CONTENT ADDRESSABLE MEMORIES AND RANDOM ACCESS MEMORIES	365/204
11	US 20030 03351 1 A1	<input checked="" type="checkbox"/>	Processor having multiple program counters and trace buffers outside an execution pipeline	712/235
12	US 20020 19445 7 A1	<input checked="" type="checkbox"/>	Memory system for ordering load and store instructions in a processor that performs out-of-order multithread execution	712/218
13	US 20020 15225 9 A1	<input checked="" type="checkbox"/>	Pre-committing instruction sequences	709/201
14	US 20020 14409 8 A1	<input checked="" type="checkbox"/>	Register rotation prediction and precomputation	712/221
15	US 20020 12922 4 A1	<input checked="" type="checkbox"/>	Method for handling 32 bit results for an out-of-order processor with A 64 bit architecture	712/209
16	US 20020 08330 4 A1	<input type="checkbox"/>	Rename finish conflict detection and recovery	712/218
17	US 20020 08329 3 A1	<input checked="" type="checkbox"/>	Register file circuitry	711/203

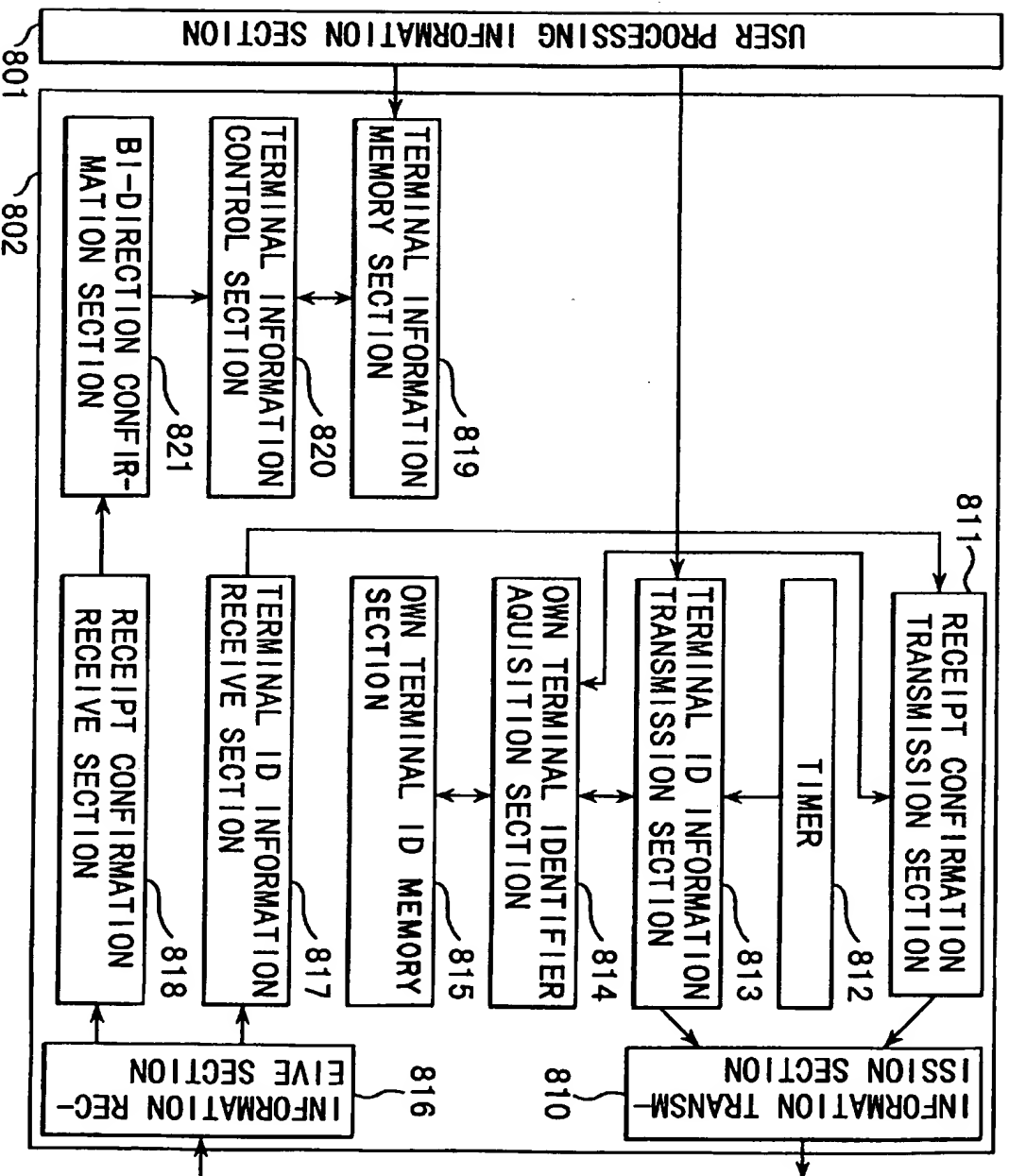
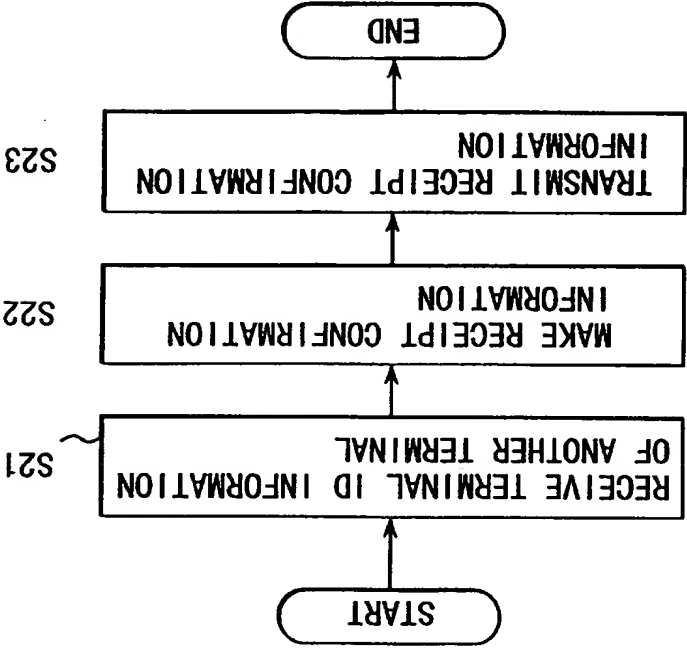


FIG. 16

	Docum ent ID	U	Title	Current OR
18	US 20020 03567 7 A1	<input checked="" type="checkbox"/>	METHOD AND APPARATUS FOR PRE-PROCESSING INSTRUCTIONS FOR A PROCESSOR	712/217
19	US 20020 02320 4 A1	<input checked="" type="checkbox"/>	Universal load address/value prediction scheme	712/239
20	US 20010 05413 9 A1	<input checked="" type="checkbox"/>	MECHANISM FOR POWER EFFICIENT PROCESSING IN A PIPELINE PROCESSOR	712/216
21	US 20010 03743 4 A1	<input checked="" type="checkbox"/>	Store to load forwarding using a dependency link file	711/146
22	US 20010 01494 1 A1	<input checked="" type="checkbox"/>	Processor having multiple program counters and trace buffers outside an execution pipeline	712/228
23	US 20010 01006 9 A1	<input checked="" type="checkbox"/>	Method for operating a non-blocking hierarchical cache throttle	711/122
24	US 67048 55 B1	<input checked="" type="checkbox"/>	Method and apparatus for reducing encoding needs and ports to shared resources in a processor	712/210
25	US 66979 39 B1	<input checked="" type="checkbox"/>	Basic block cache microprocessor with instruction history information	712/244
26	US 66842 99 B2	<input checked="" type="checkbox"/>	Method for operating a non-blocking hierarchical cache throttle	711/140
27	US 66339 71 B2	<input checked="" type="checkbox"/>	Mechanism for forward data in a processor pipeline using a single pipefile connected to the pipeline	712/218
28	US 66222 25 B1	<input checked="" type="checkbox"/>	System for minimizing memory bank conflicts in a computer system	711/158
29	US 66091 90 B1	<input checked="" type="checkbox"/>	Microprocessor with primary and secondary issue queue	712/214
30	US 66087 71 B2	<input checked="" type="checkbox"/>	Low-power circuit structures and methods for content addressable memories and random access memories	365/49
31	US 66041 90 B1	<input checked="" type="checkbox"/>	Data address prediction structure and a method for operating the same	712/207
32	US 65534 82 B1	<input checked="" type="checkbox"/>	Universal dependency vector/queue entry	712/216
33	US 65499 90 B2	<input checked="" type="checkbox"/>	Store to load forwarding using a dependency link file	711/146
34	US 65464 53 B1	<input checked="" type="checkbox"/>	Proprammable DRAM address mapping mechanism	711/5
35	US 65394 71 B2	<input checked="" type="checkbox"/>	Method and apparatus for pre-processing instructions for a processor	712/217
36	US 65230 50 B1	<input checked="" type="checkbox"/>	Integer to floating point conversion using one's complement with subsequent correction to eliminate two's complement in critical path	708/204
37	US 64991 23 B1	<input checked="" type="checkbox"/>	Method and apparatus for debugging an integrated circuit	714/724
38	US 64938 20 B2	<input checked="" type="checkbox"/>	Processor having multiple program counters and trace buffers outside an execution pipeline	712/235

TERMINAL IDENTIFIER	C1
UPDATING TIME	11:00
	C2
	10:55
	C3
	11:01
	C4
	10:58

FIG. 17

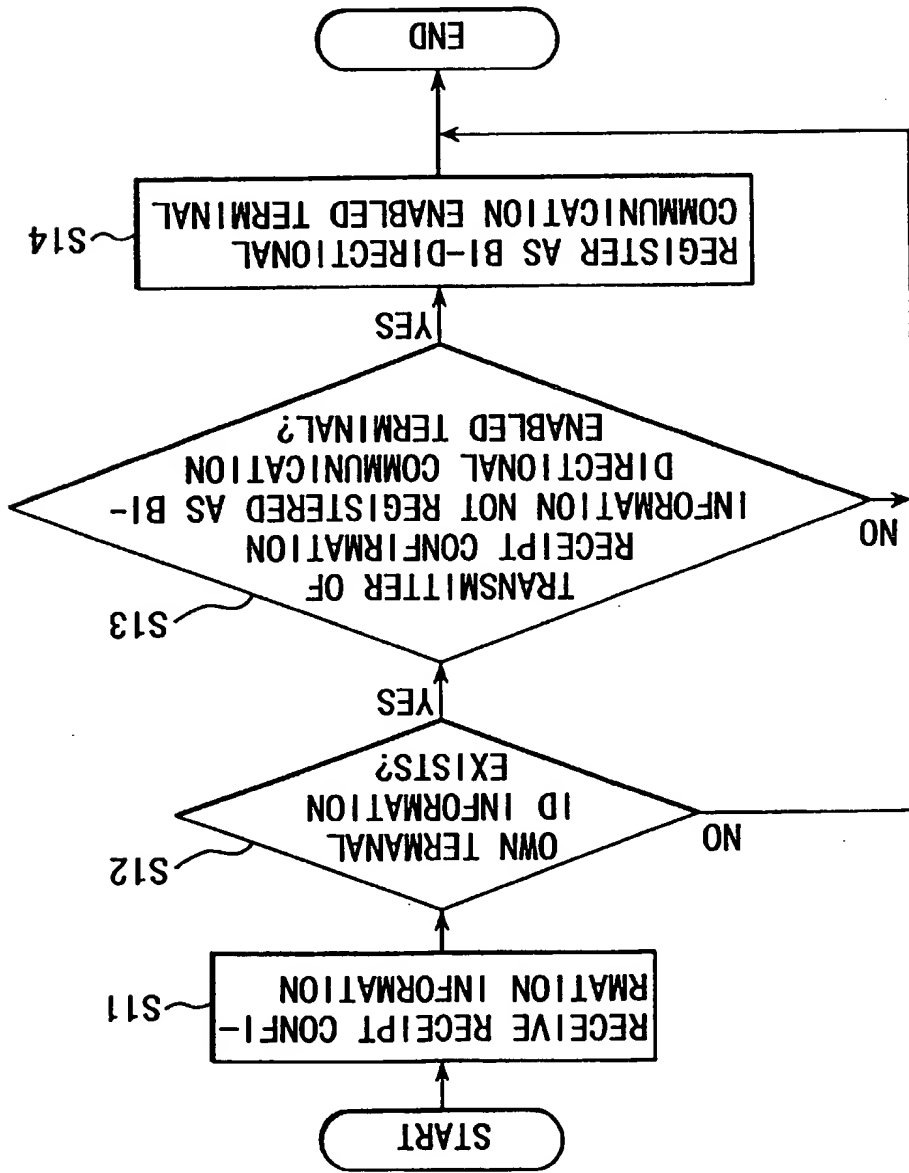


[PROCESS TO BE PERFORMED WHEN TERMINAL ID INFORMATION OF ANOTHER TERMINAL IS RECEIVED]

FIG. 19



	Docum ent ID	U	Title	Current OR
39	US 64738 37 B1	<input checked="" type="checkbox"/>	Snoop resynchronization mechanism to preserve read ordering	711/146
40	US 64738 32 B1	<input checked="" type="checkbox"/>	Load/store unit having pre-cache and post-cache queues for low latency load memory operations	711/118
41	US 64635 22 B1	<input checked="" type="checkbox"/>	Memory system for ordering load and store instructions in a processor that performs multithread execution	712/216
42	US 64271 93 B1	<input checked="" type="checkbox"/>	Deadlock avoidance using exponential backoff	711/146
43	US 64153 60 B1	<input checked="" type="checkbox"/>	Minimizing self-modifying code checks for uncacheable memory types	711/139
44	US 63935 55 B1	<input checked="" type="checkbox"/>	Rapid execution of FCMOV following FCOMI by storing comparison result in temporary register in floating point unit	712/222
45	US 63935 49 B1	<input checked="" type="checkbox"/>	Instruction alignment unit for routing variable byte-length instructions	712/204
46	US 63518 03 B1	<input checked="" type="checkbox"/>	Mechanism for power efficient processing in a pipeline processor	712/216
47	US 63398 22 B1	<input checked="" type="checkbox"/>	Using padded instructions in a block-oriented cache	712/213
48	US 63112 61 B1	<input checked="" type="checkbox"/>	Apparatus and method for improving superscalar processors	712/23
49	US 63082 59 B1	<input checked="" type="checkbox"/>	Instruction queue evaluating dependency vector in portions during different clock phases	712/214
50	US 62826 29 B1	<input checked="" type="checkbox"/>	Pipelined processor for performing parallel instruction recording and register assigning	712/23
51	US 62759 26 B1	<input checked="" type="checkbox"/>	System and method for writing back multiple results over a single-result bus and processor employing the same	712/210
52	US 62694 26 B1	<input checked="" type="checkbox"/>	Method for operating a non-blocking hierarchical cache throttle	711/140
53	US 62667 44 B1	<input checked="" type="checkbox"/>	Store to load forwarding using a dependency link file	711/146
54	US 62601 35 B1	<input checked="" type="checkbox"/>	Parallel processing unit and instruction issuing system	712/214
55	US 62498 62 B1	<input checked="" type="checkbox"/>	Dependency table for reducing dependency checking hardware	712/218
56	US 62405 09 B1	<input checked="" type="checkbox"/>	Out-of-pipeline trace buffer for holding instructions that may be re-executed following misspeculation	712/228
57	US 62405 02 B1	<input checked="" type="checkbox"/>	Apparatus for dynamically reconfiguring a processor	712/15
58	US 62197 23 B1	<input checked="" type="checkbox"/>	Method and apparatus for moderating current demand in an integrated circuit processor	710/18
59	US 62172 34 B1	<input checked="" type="checkbox"/>	Apparatus and method for processing data with an arithmetic unit	709/247
60	US 62126 29 B1	<input checked="" type="checkbox"/>	Method and apparatus for executing string instructions	712/241
61	US 62126 23 B1	<input checked="" type="checkbox"/>	Universal dependency vector/queue entry	712/216



[PROCESS TO BE PERFORMED WHEN RECEIPT  
CONFIRMATION INFORMATION IS RECEIVED]

FIG. 18

	Docum ent ID	U	Title	Current OR
62	US 62126 22 B1	<input checked="" type="checkbox"/>	Mechanism for load block on store address generation	712/216
63	US 62126 02 B1	<input checked="" type="checkbox"/>	Cache tag caching	711/122
64	US 62090 84 B1	<input checked="" type="checkbox"/>	Dependency table for reducing dependency checking hardware	712/233
65	US 61957 44 B1	<input checked="" type="checkbox"/>	Unified multi-function operation scheduler for out-of-order execution in a superscaler processor	712/215
66	US 61924 62 B1	<input checked="" type="checkbox"/>	Superscalar microprocessor including a load/store unit, decode units and a reorder buffer to detect dependencies between access to a stack cache and a data cache	712/23
67	US 61856 75 B1	<input checked="" type="checkbox"/>	Basic block oriented trace cache utilizing a basic block sequence buffer to indicate program order of cached basic blocks	712/238
68	US 61822 10 B1	<input checked="" type="checkbox"/>	Processor having multiple program counters and trace buffers outside an execution pipeline	712/235
69	US 61548 15 A	<input checked="" type="checkbox"/>	Non-blocking hierarchical cache throttle	711/140
70	US 61548 12 A	<input checked="" type="checkbox"/>	Method for inhibiting thrashing in a multi-level non-blocking cache system	711/122
71	US 61483 71 A	<input checked="" type="checkbox"/>	Multi-level non-blocking cache system with inhibiting thrashing	711/122
72	US 61417 34 A	<input checked="" type="checkbox"/>	Method and apparatus for optimizing the performance of LDxL and STxC interlock instructions in the context of a write invalidate protocol	711/144
73	US 61417 21 A	<input checked="" type="checkbox"/>	Method of asynchronous memory access	711/1
74	US 61227 27 A	<input checked="" type="checkbox"/>	Symmetrical instructions queue for high clock frequency scheduling	712/214
75	US 61192 13 A	<input checked="" type="checkbox"/>	Method for addressing data having variable data width using a fixed number of bits for address and width defining fields	711/202
76	US 61120 19 A	<input checked="" type="checkbox"/>	Distributed instruction queue	712/214
77	US 61087 69 A	<input checked="" type="checkbox"/>	Dependency table for reducing dependency checking hardware	712/216
78	US 60818 73 A	<input checked="" type="checkbox"/>	In-line bank conflict detection and resolution in a multi-ported non-blocking cache	711/131
79	US 60816 56 A	<input checked="" type="checkbox"/>	Method for deriving a double frequency microprocessor from an existing microprocessor	716/3
80	US 60584 66 A	<input checked="" type="checkbox"/>	System for allocation of execution resources amongst multiple executing processes	712/15
81	US 60527 75 A	<input checked="" type="checkbox"/>	Method for non-intrusive cache fills and handling of load misses	712/215
82	US 60473 69 A	<input checked="" type="checkbox"/>	Flag renaming and flag masks within register alias table	712/217
83	US 60353 74 A	<input checked="" type="checkbox"/>	Method of executing coded instructions in a multiprocessor having shared execution resources including active, nap, and sleep states in accordance with cache miss latency	711/118
84	US 60063 26 A	<input checked="" type="checkbox"/>	Apparatus for restraining over-eager load boosting in an out-of-order machine using a memory disambiguation buffer for determining dependencies	712/217

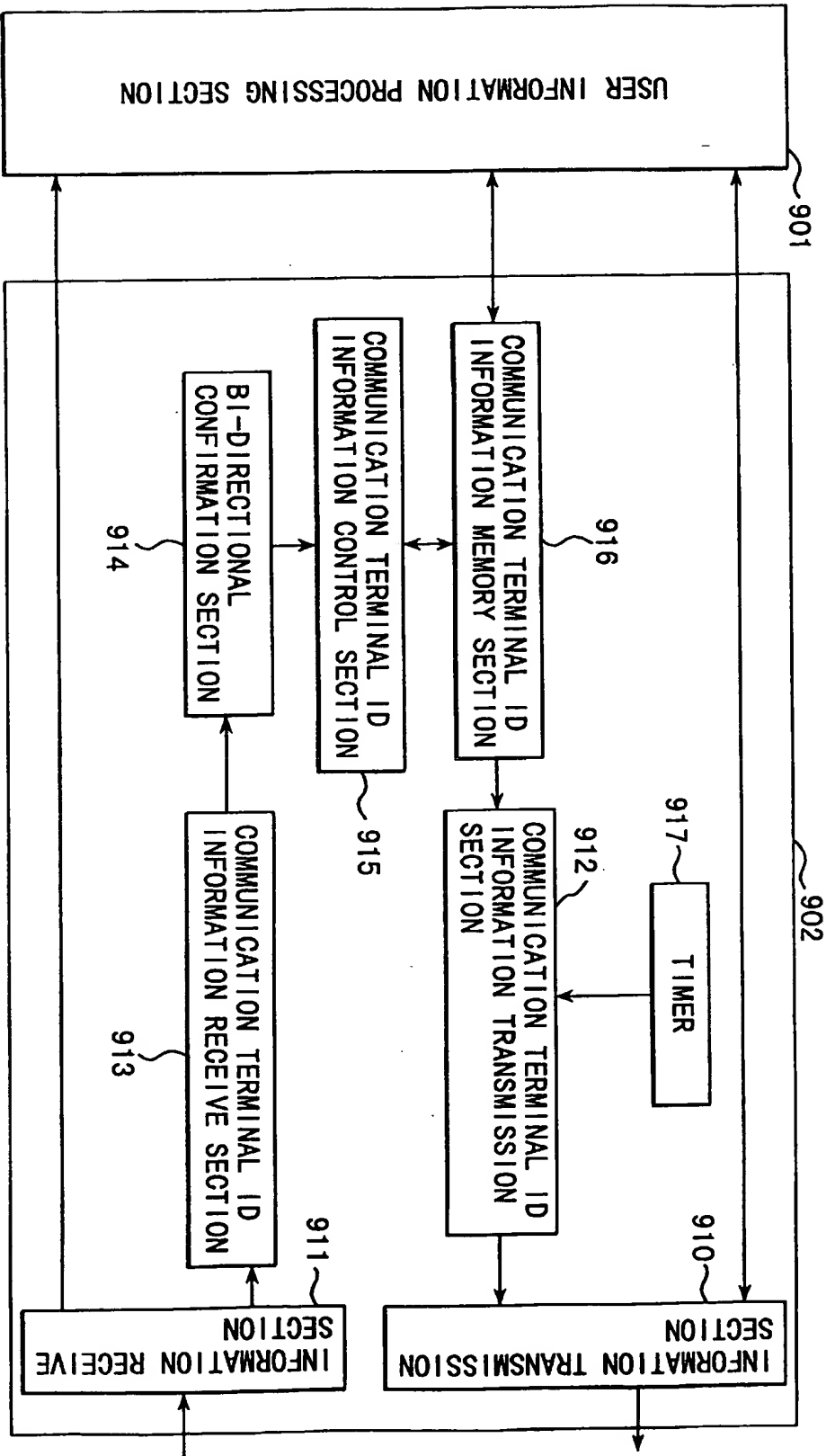


FIG. 20

	Docum ent ID	U	Title	Current OR
85	US 60063 24 A	<input checked="" type="checkbox"/>	High performance superscalar alignment unit	712/204
86	US 59997 27 A	<input checked="" type="checkbox"/>	Method for restraining over-eager load boosting using a dependency color indicator stored in cache with both the load and store instructions	712/225
87	US 59957 27 A	<input checked="" type="checkbox"/>	Video decompression	709/247
88	US 59875 98 A	<input checked="" type="checkbox"/>	Method and system for tracking instruction progress within a data processing system	712/227
89	US 59875 94 A	<input checked="" type="checkbox"/>	Apparatus for executing coded dependent instructions having variable latencies	712/216
90	US 59845 12 A	<input checked="" type="checkbox"/>	Method for storing video information	709/219
91	US 59833 42 A	<input checked="" type="checkbox"/>	Superscalar microprocessor employing a future file for storing results into multiportion registers	712/218
92	US 59788 64 A	<input checked="" type="checkbox"/>	Method for thermal overload detection and prevention for an intergrated circuit processor	710/18
93	US 59745 31 A	<input checked="" type="checkbox"/>	Methods and systems of stack renaming for superscalar stack-based data processors	712/202
94	US 59745 23 A	<input checked="" type="checkbox"/>	Mechanism for efficiently overlapping multiple operand types in a microprocessor	712/23
95	US 59681 69 A	<input checked="" type="checkbox"/>	Superscalar microprocessor stack structure for judging validity of predicted subroutine return addresses	712/239
96	US 59631 54 A	<input checked="" type="checkbox"/>	Technique for decoding variable and fixed length codes	341/67
97	US 59481 06 A	<input checked="" type="checkbox"/>	System for thermal overload detection and prevention for an integrated circuit processor	713/501
98	US 59308 19 A	<input checked="" type="checkbox"/>	Method for performing in-line bank conflict detection and resolution in a multi-ported non-blocking cache	711/131
99	US 59304 91 A	<input checked="" type="checkbox"/>	Identification of related instructions resulting from external to internal translation by use of common ID field for each group	712/209
100	US 59220 69 A	<input checked="" type="checkbox"/>	Reorder buffer which forwards operands independent of storing destination specifiers therein	712/217
101	US 58988 53 A	<input checked="" type="checkbox"/>	Apparatus for enforcing true dependencies in an out-of-order processor	712/216
102	US 58900 08 A	<input checked="" type="checkbox"/>	Method for dynamically reconfiguring a processor	712/15
103	US 58871 52 A	<input checked="" type="checkbox"/>	Load/store unit with multiple oldest outstanding instruction pointers for completing store and load/store miss instructions	712/217
104	US 58840 61 A	<input checked="" type="checkbox"/>	Apparatus to perform source operand dependency analysis perform register renaming and provide rapid pipeline recovery for a microprocessor capable of issuing and executing multiple instructions out-of-order in a single processor cycle	712/217
105	US 58840 59 A	<input checked="" type="checkbox"/>	Unified multi-function operation scheduler for out-of-order execution in a superscalar processor	712/215
106	US 58782 73 A	<input checked="" type="checkbox"/>	System for microprogrammable state machine in video parser disabling portion of processing stages responsive to sequence.sub.-- end token generating by token generator responsive to received data	710/5

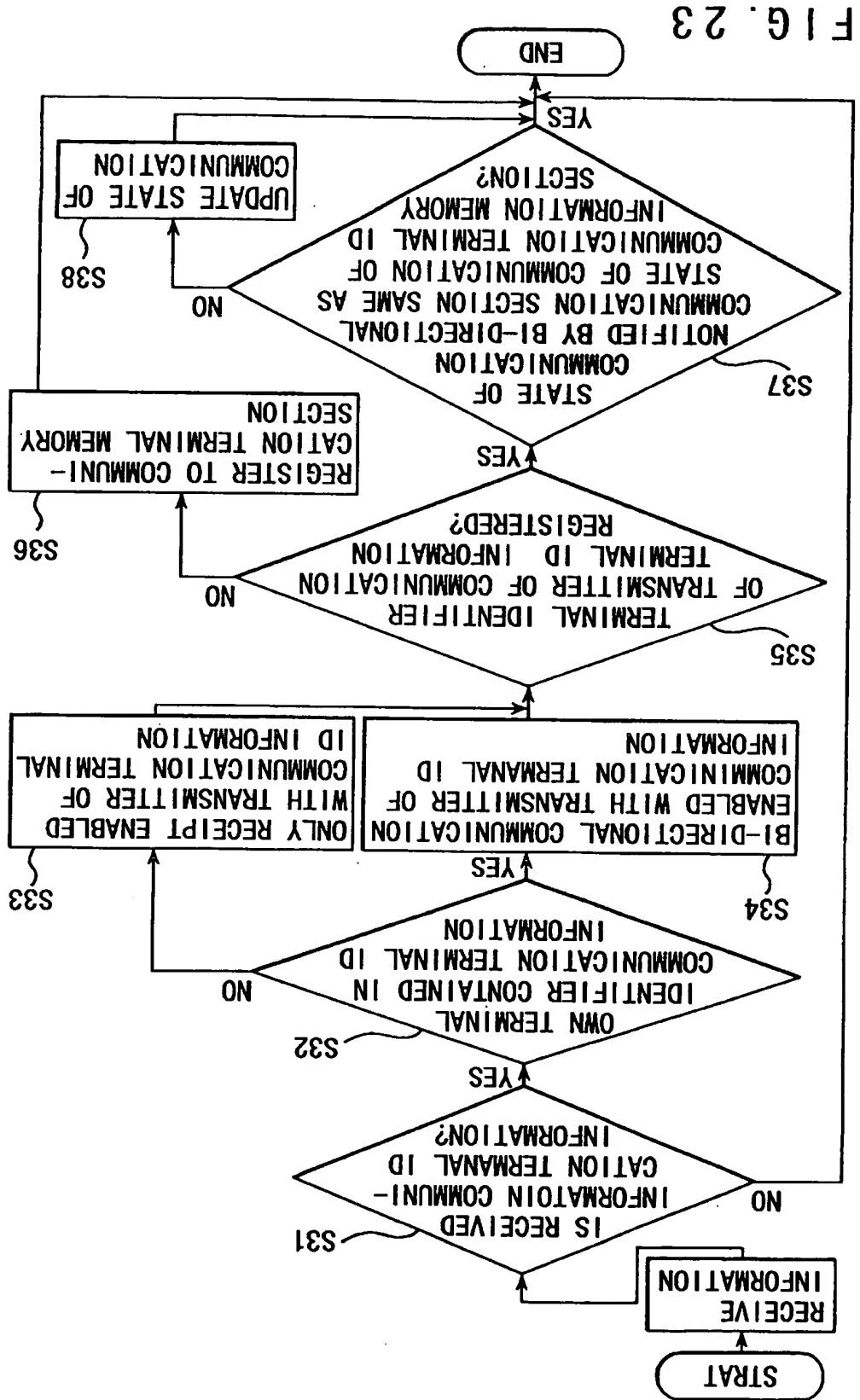
OWN TERMINAL IDENTIFIER	LIST OF RECEIPT ENABLED TERMINAL	LIST OF BI-DIRECTIONAL COMMUNICATION ENABLED TERMINALS
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FIG. 21

TERMINAL IDENTIFIER	STATE OF COMMUNICATION	PERIPHERAL TERMINAL INFORMATION	UPDATING TIME
C1	BI-DIRECTION	C2 C4 C8	11:00
C2	BI-DIRECTION	C1 C3 C8	10:55
C3	BI-DIRECTION	C2 C4	11:01
C4	RECEIPT	C1 C3 C5	10:58

FIG. 22

	Docum ent ID	U	Title	Current OR
107	US 58705 80 A	<input checked="" type="checkbox"/>	Decoupled forwarding reorder buffer configured to allocate storage in chunks for instructions having unresolved dependencies	712/218
108	US 58505 33 A	<input checked="" type="checkbox"/>	Method for enforcing true dependencies in an out-of-order processor	712/216
109	US 58484 33 A	<input checked="" type="checkbox"/>	Way prediction unit and a method for operating the same	711/137
110	US 58482 87 A	<input checked="" type="checkbox"/>	Superscalar microprocessor including a reorder buffer which detects dependencies between accesses to a pair of caches	712/23
111	US 58357 92 A	<input checked="" type="checkbox"/>	Token-based adaptive video processing arrangement	710/68
112	US 58357 45 A	<input checked="" type="checkbox"/>	Hardware instruction scheduler for short execution unit latencies	712/215
113	US 58322 97 A	<input checked="" type="checkbox"/>	Superscalar microprocessor load/store unit employing a unified buffer and separate pointers for load and store operations	710/5
114	US 58322 49 A	<input checked="" type="checkbox"/>	High performance superscalar alignment unit	712/204
115	US 58290 07 A	<input checked="" type="checkbox"/>	Technique for implementing a swing buffer in a memory array	711/5
116	US 58289 07 A	<input checked="" type="checkbox"/>	Token-based adaptive video processing arrangement	710/68
117	US 58288 86 A	<input checked="" type="checkbox"/>	Compiling apparatus and method for promoting an optimization effect of a program	717/159
118	US 58288 74 A	<input checked="" type="checkbox"/>	Past-history filtered branch prediction	712/240
119	US 58260 89 A	<input checked="" type="checkbox"/>	Instruction translation unit configured to translate from a first instruction set to a second instruction set	717/146
120	US 58225 74 A	<input checked="" type="checkbox"/>	Functional unit with a pointer for mispredicted resolution, and a superscalar microprocessor employing the same	712/233
121	US 58225 58 A	<input checked="" type="checkbox"/>	Method and apparatus for predecoding variable byte-length instructions within a superscalar microprocessor	712/213
122	US 58218 85 A	<input checked="" type="checkbox"/>	Video decompression	341/67
123	US 58190 59 A	<input checked="" type="checkbox"/>	Predecode unit adapted for variable byte-length instruction set processors and method of operating the same	712/213
124	US 58190 57 A	<input checked="" type="checkbox"/>	Superscalar microprocessor including an instruction alignment unit with limited dispatch to decode units	712/204
125	US 58130 33 A	<input checked="" type="checkbox"/>	Superscalar microprocessor including a cache configured to detect dependencies between accesses to the cache and another cache	711/144
126	US 58058 76 A	<input checked="" type="checkbox"/>	Method and system for reducing average branch resolution time and effective misprediction penalty in a processor	712/234
127	US 58058 53 A	<input checked="" type="checkbox"/>	Superscalar microprocessor including flag operand renaming and forwarding apparatus	712/218
128	US 58019 73 A	<input checked="" type="checkbox"/>	Video decompression	708/203
129	US 57987 19 A	<input checked="" type="checkbox"/>	Parallel Huffman decoder	341/67





	Docum ent ID	U	Title	Current OR
130	US 57874 74 A	<input checked="" type="checkbox"/>	Dependency checking structure for a pair of caches which are accessed from different pipeline stages of an instruction processing pipeline	711/138
131	US 57817 53 A	<input checked="" type="checkbox"/>	Semi-autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for speculative and out-of-order execution of complex instructions	712/218
132	US 57782 45 A	<input checked="" type="checkbox"/>	Method and apparatus for dynamic allocation of multiple buffers in a processor	712/23
133	US 57686 29 A	<input checked="" type="checkbox"/>	Token-based adaptive video processing arrangement	710/68
134	US 57686 10 A	<input checked="" type="checkbox"/>	Lookahead register value generator and a superscalar microprocessor employing same	712/23
135	US 57685 75 A	<input checked="" type="checkbox"/>	Semi-Autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for sepculative and out-of-order execution of complex instructions	712/228
136	US 57650 35 A	<input checked="" type="checkbox"/>	Recorder buffer capable of detecting dependencies between accesses to a pair of caches	712/216
137	US 57649 46 A	<input checked="" type="checkbox"/>	Superscalar microprocessor employing a way prediction unit to predict the way of an instruction fetch address and to concurrently provide a branch prediction address corresponding to the fetch address	712/239
138	US 57404 60 A	<input checked="" type="checkbox"/>	Arrangement for processing packetized data	348/473
139	US 57376 29 A	<input checked="" type="checkbox"/>	Dependency checking and forwarding of variable width operands	712/23
140	US 57271 77 A	<input checked="" type="checkbox"/>	Reorder buffer circuit accommodating special instructions operating on odd-width results	712/218
141	US 57218 55 A	<input checked="" type="checkbox"/>	Method for pipeline processing of instructions by controlling access to a reorder buffer using a register file outside the reorder buffer	712/218
142	US 57173 94 A	<input checked="" type="checkbox"/>	Method and apparatus for encoding and decoding data	341/51
143	US 57037 93 A	<input checked="" type="checkbox"/>	Video decompression	382/232
144	US 56665 06 A	<input checked="" type="checkbox"/>	Apparatus to dynamically control the out-of-order execution of load/store instructions in a processor capable of dispatchng, issuing and executing multiple instructions in a single processor cycle	712/216
145	US 56492 25 A	<input checked="" type="checkbox"/>	Resynchronization of a superscalar processor	712/23
146	US 56340 26 A	<input checked="" type="checkbox"/>	Source identifier for result forwarding	712/217
147	US 56320 23 A	<input checked="" type="checkbox"/>	Superscalar microprocessor including flag operand renaming and forwarding apparatus	712/218
148	US 56301 49 A	<input checked="" type="checkbox"/>	Pipelined processor with register renaming hardware to accommodate multiple size registers	712/217
149	US 56257 89 A	<input checked="" type="checkbox"/>	Apparatus for source operand dependency analyses register renaming and rapid pipeline recovery in a microprocessor that issues and executes multiple instructions out-of-order in a single cycle	712/217

```

graph TD
    1103[FROM NETWORK] --> 1104[PACKET RECEIVE SECTION]
    1104 --> 1105[RECEIVED PACKET DETERMINATION SECTION]
    1106[PACKET ID MEMORY SECTION] <--> 1105
    1105 --> 1107[PACKET TRANSMISSION SECTION]
    1105 --> 1108[PACKET RE-TRANSMISSION SECTION]
    1107 --> 1109[PACKET ID IMPARTING SECTION]
    1106 --> 1109
    1109 --> 1107
    1107 --> 1110[TO NETWORK]
    1111[USER INFORMATION PROCESSING SECTION] --> 1106
    1111 --> 1109
  
```

	Docum ent ID	U	Title	Current OR
150	US 56196 62 A	<input checked="" type="checkbox"/>	Memory reference tagging	712/216
151	US 56153 50 A	<input checked="" type="checkbox"/>	Apparatus to dynamically control the out-of-order execution of load-store instructions in a processor capable of dispatching, issuing and executing multiple instructions in a single processor cycle	712/218
152	US 55903 52 A	<input checked="" type="checkbox"/>	Dependency checking and forwarding of variable width operands	712/23
153	US 55862 78 A	<input checked="" type="checkbox"/>	Method and apparatus for state recovery following branch misprediction in an out-of-order microprocessor	712/235
154	US 55817 19 A	<input checked="" type="checkbox"/>	Multiple block line prediction	712/207
155	US 55641 18 A	<input checked="" type="checkbox"/>	Past-history filtered branch prediction	712/240
156	US 55465 97 A	<input checked="" type="checkbox"/>	Ready selection of data dependent instructions using multi-cycle cams in a processor performing out-of-order instruction execution	712/23
157	US 55198 41 A	<input checked="" type="checkbox"/>	Multi instruction register mapper	711/202
158	US 54715 93 A	<input checked="" type="checkbox"/>	Computer processor with an efficient means of executing many instructions simultaneously	712/235
159	US 54712 07 A	<input checked="" type="checkbox"/>	Compression of palettized images and binarization for bitwise coding of M-ary alphabets therefor	341/107
160	US 54044 70 A	<input checked="" type="checkbox"/>	Information processing apparatus for processing instructions by out-of-order execution	712/217
161	US 51504 69 A	<input checked="" type="checkbox"/>	System and method for processor pipeline control by selective signal deassertion	712/244
162	US 51194 95 A	<input checked="" type="checkbox"/>	Minimizing hardware pipeline breaks using software scheduling techniques during compilation	717/153
163	US 49657 24 A	<input type="checkbox"/>	Compiler system using reordering of microoperations to eliminate interlocked instructions for pipelined processing of assembler source program	717/160

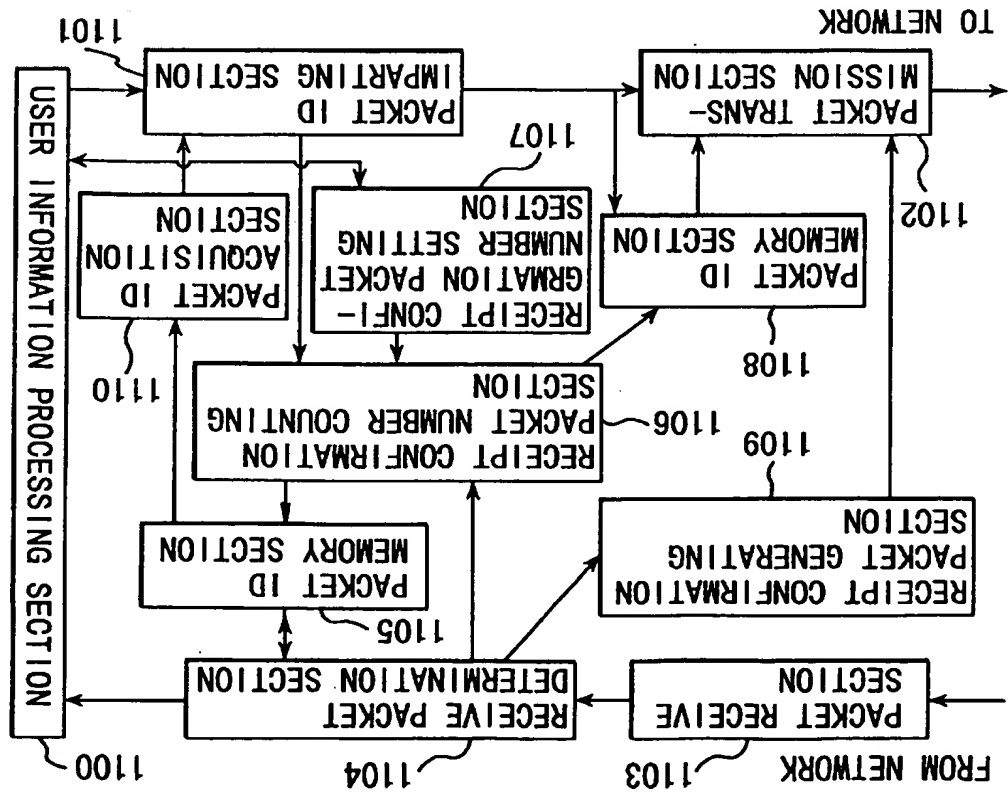


FIG. 25

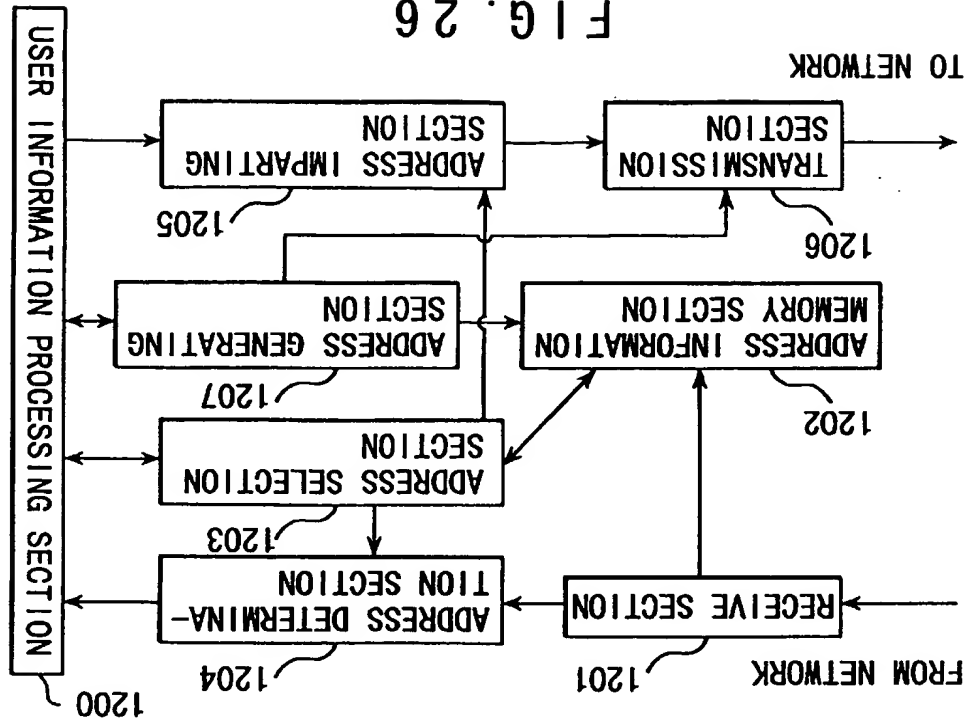


FIG. 26